AMENDMENTS TO THE CLAIMS

Please amend the claims as indicated in the following listing of all claims:

1. (Original) A clock recovery circuit comprising:
a phase detector circuit coupled to generate a difference signal indicating a phase difference between an incoming data stream and a delayed clock signal;
an oscillator circuit responsive to a control signal derived from the difference signal to generate an output clock signal variable according to the control signal; and
a clock delay circuit coupled to receive a delay control signal derived from the difference signal and to receive the output clock signal, the clock delay circuit coupled to provide as the delayed clock signal the output clock signal delayed according to the delay control signal.

2. (Previously presented) The clock recovery circuit as recited in claim 1 further comprising a loop filter circuit coupled to receive the difference signal and supply a filtered output as the control signal.

3. (Original) The clock recovery circuit as recited in claim 1 wherein the control signal for the oscillator circuit is used as the delay control signal.

4. (Previously presented) The clock recovery circuit as recited in claim 1 further comprising a delay control filter circuit coupled to receive the difference signal and generate the delay control signal based thereon.

5. (Original) The clock recovery circuit as recited in claim 1 wherein the clock delay circuit is a voltage controlled delay circuit.

6. (Original) The clock recovery circuit as recited in claim 1 wherein the clock delay circuit comprises multiple stages.

7. (Previously presented) The clock recovery circuit as recited in claim 6 wherein a delay period from one stage to a next stage in the clock delay circuit is less than one period of the output clock signal.

8. (Currently amended) ~~The clock recovery circuit as recited in claim 7 further comprising:~~ A clock recovery circuit comprising:

a phase detector circuit coupled to generate a difference signal indicating a phase difference between an incoming data stream and a delayed clock signal;

an oscillator circuit responsive to a control signal derived from the difference signal to generate an output clock signal variable according to the control signal;

a clock delay circuit coupled to receive a delay control signal derived from the difference signal and to receive the output clock signal, the clock delay circuit coupled to provide as the delayed clock signal the output clock signal delayed according to the delay control signal;

a plurality of serially coupled registers, including at least a first register and a last register and wherein the first register is coupled to receive data synchronized to the delayed clock signal and is further coupled to receive a clock signal from the clock delay circuit that is less delayed than the delayed clock signal;

wherein the clock delay circuit comprises multiple stages;

wherein a delay period from one stage to a next stage in the clock delay circuit is less than one period of the output clock signal;

and wherein the last register is coupled to the output clock signal and to receive data from a previous one of the plurality of serially coupled registers, thereby providing out of the last register data retimed to the output clock signal.

9. (Previously presented) The clock recovery circuit as recited in claim 8 further comprising at least one intermediate register serially coupled between the first and last registers, each of the plurality of serially coupled registers receiving a successively less delayed clock signal.

10. (Original) The clock recovery circuit as recited in claim 1 further comprising a data recovery circuit.

11. (Original) The clock recovery circuit as recited in claim 1 wherein the oscillator circuit is a voltage controlled oscillator.

12. (Original) The clock recovery circuit as recited in claim 1 further comprising means for retiming the incoming data signal from the delayed clock signal to the output clock signal.

13. (Original) The clock recovery circuit as recited in claim 1 further comprising:

a first in first out (FIFO) memory coupled to write data into the FIFO memory with the delayed clock signal and to read data out of the FIFO memory with the output clock signal, thereby retiming data to the output clock signal.

14. (Original) The clock recovery circuit as recited in claim 1 having a closed loop response without an explicit zero.

15. (Original) A method of recovering a clock signal from an input data stream comprising:

determining a phase difference between the input data stream and a delayed clock signal and generating a difference signal indicative thereof;

generating a control signal from the difference signal to control an oscillator;

generating in the oscillator an output clock signal that varies according to the control signal; and

receiving the output clock signal in a delay circuit and generating the delayed clock signal from the output clock signal according to a delay control signal derived from the difference signal.

16. (Original) The method as recited in claim 15 further comprising using the control signal for the oscillator as the delay control signal.

17. (Previously presented) The method as recited in claim 15 further comprising generating the delay control signal in a delay filter circuit separate from the control signal.

18. (Original) The method as recited in claim 15 further comprising providing input data from the input data stream that is synchronized to the delayed clock signal and retiming the input data from the delayed clock signal to the output clock signal.

19. (Previously presented) The method as recited in claim 18 further comprising generating the delayed clock signal in a plurality of stages in the delay circuit and wherein a delay period from one stage to a next stage in the delay circuit is less than one period of the output clock signal.

20. (Currently Amended) The method as recited in claim 19 wherein retiming the input data further comprises:

providing data synchronized to the delayed clock signal to a first register of a plurality of ~~sucessively~~ successively coupled registers;

clocking the first register with a clock signal from the delay circuit that is less delayed than the delayed clock signal;

supplying a last register of the plurality of successively coupled registers with data from a previous register of the plurality of successively coupled registers; and

clocking the last register of the plurality of successively coupled registers with the output clock signal to thereby retime data from the delayed clock signal to the output clock signal.

21. (Original) The method as recited in claim 20 wherein the previous register is the first register.

22. (Previously presented) The method as recited in claim 18 further comprising:

writing data synchronized to the delayed clock signal into a memory;

reading data from the memory with the output clock signal to thereby retime the data from the delayed clock signal to the output clock signal.

23. (Original) The method as recited in claim 22 wherein the memory is a first in first out memory.

24. (Previously presented) An apparatus comprising:

means for detecting a phase difference between an incoming data stream and a delayed clock signal and generating a difference signal indicative thereof;

means for generating a control signal according to the difference signal;

means for generating a clock signal that varies according to the control signal; and

means for generating the delayed clock signal from the clock signal according to a delay control signal derived from the difference signal.

25. (Original) The apparatus as recited in claim 24 further comprising means for retiming data from the delayed clock signal to the clock signal.